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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/940,262	08/28/2001	William D. Corti	FIS920010247US1	5463

7590 03/18/2004

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EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 03/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/940,262	CORTI ET AL.	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-21* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1 – 20, drawn to a method of translating an address of one type of memory device to an address for a different type of memory device, classified in class 711, subclass 202.

   II. Claim 21, drawn to a method of translating memory locations between memory arrays with different array dimensions with a specific dimensional size relationship, classified in class 711, subclass 202.

Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I does not require the translation between arrays with different dimensional structures, while the invention II does not require the translation of addresses for different types of devices.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

During a telephone conversation with Applicant's attorney of record, Daryl Neff, on March 10, 2004 a provisional election was made without traverse to prosecute the invention of

group I, claims 1 – 20. Affirmation of this election must be made by applicant in replying to this Office action. Claim 21 is withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 7 and its dependant claims 8 – 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 recites the limitation "said initial address bits" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 6 – 7 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Krause *et al.*(US Patent No. 5,959,911, hereinafter "Krause').

6. With respect to claims 6 and 7, Krause discloses a method for decoding a memory array address for an embedded DRAM (eDRAM) device (figure 1, 10, col.2 , line 35), the eDRAM device configured for operation with an SDRAM memory manager (col. 2, line 44, also note that RAM devices 12 – 16, are embedded in the same chip as the control circuits), the method comprising:

receiving a set of row address bits from the memory manager at a first time (col. 6, lines 30 – 31);

receiving a set of initial column address bits from the memory manager at a later time (col. 6, lines 29 – 31);

translating said set of initial column address bits to a set of translated column address bits (col. 6, lines 37 – 39); and

simultaneously using said set of row address bits and said set of translated column address bits to access a desired memory location in the eDRAM device (col. 6, lines 21 – 42, both sets of address bits are required to be used simultaneously to write to a desired location in each memory bank);

wherein said desired memory location in the eDRAM device has a row address corresponding to the value of said set of row address bits and a column address corresponding to the value of said set of translated column address bits.

7. With respect to claim 7, a first subset of said initial address bits (col. 6, lines 37 – 39, column address bits changed by the increment operation) is used to generate said translated column address bits; and

a second subset of initial address bits (column address bits not changed by the increment operation) is used to identify a specific location within an eDRAM column corresponding to said translated column address bits (column address bits, including the ones in the second subset, in conjunction with row address bits are used to identify a specific location within a column that corresponds to the incremented column address).

8. Claims 1 – 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Olarig *et al.*(US Patent No. 6,260,127, hereinafter "Olarig').

9. With respect to claims 1 – 2, and 6, Olarig discloses a method for decoding a memory array address for an embedded DRAM (eDRAM) device (figure 3, 320, col. 8, lines 53 – 55, EDO devices are embedded in a memory module, they are also embedded in a chip), the eDRAM device configured for operation with an SDRAM memory manager (col. 8, lines 1 – 2), the method comprising:

receiving a set of row address bits from the memory manager at a first time (figures 6 and 11, row address is received during the bank activate command phase);

receiving a set of initial column address bits from the memory manager at a later time (figures 6, 7 and 11, column address bits are received during the r/w command phase) ;

translating said set of initial column address bits to a set of translated column address bits (figures 6 and 7); and

simultaneously using said set of row address bits and said set of translated column address bits to access a desired memory location in the eDRAM device;

wherein said desired memory location in the eDRAM device has a row address corresponding to the value of said set of row address bits and a column address corresponding to the value of said set of translated column address bits.

10. With respect to claims 3 and 7, a first subset of said initial address bits is used to generate said translated column address bits (figures 6 and 7, SDRAM compliant addresses are used to generate EDO compatible addresses) ; and

a second subset of initial address bits is used to identify a specific location within a memory array column corresponding to said translated column address bits (SDRAM column address bits along with row address bits are use to identify a specific location within a column corresponding to the translated address bits).

11. With respect to claims 4 and 8, said memory manager processes memory address information in accordance with a first memory page structure (figure 6, SDRAM memory page structure); and

the memory array is configured in accordance with a second memory page structure (EDO page structure);

wherein a memory page structure is defined by the number of columns included in a given row, and the number of storage locations located at each column in said given row.

12. With respect to claims 5 and 9, said first memory page structure and said second memory page structure contain an unequal number of columns (figure 6, the first structure has a 10-bit column address and the second structure has an 11-bit column address, i.e. twice as many columns); and

said first and second memory page structures contain an equal number of storage locations (the number of storage locations are equal since the total number of address bits in both structures are equal).

13. With respect to claims 10 and 15 – 16, Olarig discloses a computer memory system, comprising:

an SDRAM memory controller (figure 8, 200);

an embedded DRAM (eDRAM) device integrated with said SDRAM memory controller (EDO RAM device is integrate with the memory controller in a memory subsystem, which is in turn integrated into a computer system) ; and

an address decoding apparatus for translating a memory address generated by said SDRAM memory controller to a translated memory address in said eDRAM device (figures 6 and 7).

wherein said address decoding apparatus further comprises:

a register for receiving a set of row address bits from the memory controller at a first time (figures 6, 7 and 11, and col. 24, lines 60 – 67, column and row addresses are latched);

a counter for receiving a set of initial column address bits from the memory controller at a later time (figures 6, 7 and 11); and

a broadside address register for simultaneously receiving a first subset of said set of initial column address bits and said row address bits (figures 6 and 7, address presented to EDO at CAS consists of some row address bits and column address bits);

wherein said first subset of said set of initial column address bits defines a translated column address for the eDRAM device.

14. With respect to claims 11 and 17, the system further comprises a:

a multiplexing device (col. 9, lines 54 – 56) for receiving a second subset of said set of initial column address bits;

wherein said second subset of said set of initial column address bits corresponds to a specific storage location segment within said translated column address (figure 6, there are many subsets of column address bits that corresponds to a specific location segment within the translated column address, for example the address bit A0 corresponds to a specific location segment and address bits A0 and A1 correspond to a specific location segment as well).

15. With respect to claims 12 and 18, the eDRAM device includes a first eDRAM module coupled with a second eDRAM module (figure 7, EDO DIMM 0 and DIMM 1, see also figure 8 320a-d).

16. With respect to claim 13 and 19, the system further comprises:

steering logic for determining in which of said first and second eDRAM modules said specific storage location segment is contained (table 4, the address translator determines in which of the first or the second EDO module the addressed storage location segment is contained based on the translated address which is dependant on the translation scheme, see the two 2 to 1 example translation schemes in the table).

17. With respect to claims 14 and 20, an input to said steering logic comprises a third subset of said set of initial column address bits (figure 6, column address bits A0 – A2).

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Dowling (US Patent No. 6,226,738) discloses a computer system where an embedded DRAM module can be used with a standard SDRAM controller. Zhang et al. (A Programmable BIST for Embedded SDRAM, IEEE, 2001) and Yamauchi et al (Design Methodology of Embedded DRAM with Virtual-Socket Architecture, IEEE Journal of Solid State Circuits, vol. 36, January 2001) disclose an integrated embedded DRAM and SDRAM controller. Hwang et al. (US Patent No. 5,901,304) disclose another system where an SDRAM controller is integrated with embedded DRAM modules. Manseau (US Patent No. 6,629,219), Kurjanowicz et al. (US Patent No. 6,584,036), and Sarma et al (US Patent No. 5,918,242) disclose other systems that translate addresses from one format to another.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (703) 305-3845. The examiner can normally be reached on M-F, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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March 12, 2004

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